N-Channel 100V(D-S) MOSFET

GENERAL DESCRIPTION

The MEE4294HP-G is a N-Channel enhancement mode power field effect transistor, using Force-MOS patented Extended Trench Gate (ETG) technology. This advanced technology is especially tailored to minimize on state resistance and gate charge, and enhance avalanche capability. These devices are particularly suited for medium voltage application such as charger, adapter, notebook computer power management and other lighting dimming powered circuits, and low in-line power loss that are needed in a very small outline surface mount package.

FEATURES

- RDS(ON)≦10mΩ@VGS=10V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

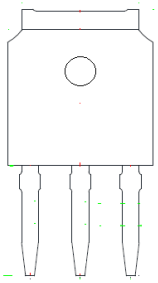
APPLICATIONS

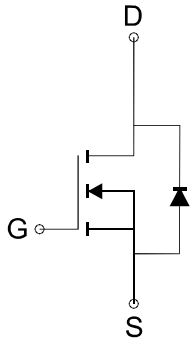
- Power Management
- Synchronous Rectification
- Load Switch

PIN CONFIGURATION

(TO-251)

Top View





N-Channel MOSFET

Ordering Information:MEE4294HP-G (Pb-free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DSS}	100	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current*	T_C=25℃	I_D	53	A
	T_C=70℃		42	
	T_A=25℃		11.5	
	T_A=70℃		9.2	
Pulsed Drain Current		I_{DM}	212	A
Maximum Power Dissipation*	T_C=25℃	P_D	59.5	W
	T_C=70℃		38.1.	
	T_A=25℃		2.78	
	T_A=70℃		1.78	
Operating Junction and Storage Temperature Range		TJ, Tstg	-55 to 150	℃
Thermal Resistance-Junction to Case *		$R_{\theta JC}$	2.1	℃/W
Junction-to-Ambient Thermal Resistance*		$R_{\theta JA}$	45	

* The device mounted on 1in^2 FR4 board with 2 oz copper

* Chip silicon limitation current is 100A

Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	100			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	2		4	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=100V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance [a]	V_{GS}=10V, I_D= 20A		8	10	mΩ
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V			1	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=50V,V_{GS}=10V, I_D=20A		49.2		nC
Qg	Total Gate Charge	V_{DS}=50V,V_{GS}=4.5V, I_D=20A		26.8		
Qgs	Gate-Source Charge			16		
Qgd	Gate-Drain Charge			10.3		
Ciss	Input capacitance	V_{DS}=30V,V_{GS}=0V, f=1.0MHz		2819		pF
Coss	Output Capacitance			868		
Crss	Reverse Transfer Capacitance			55		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=50V, R_L =2.5Ω V_{GS}=10V,R_G=6Ω I_D=20A		25.9		ns
t_r	Turn-On Rise Time			69.5		
$t_{d(off)}$	Turn-Off Delay Time			57.2		
t_f	Turn-Off Fall Time			24		

Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Force mos reserves the right to improve product design, functions and reliability without notice.

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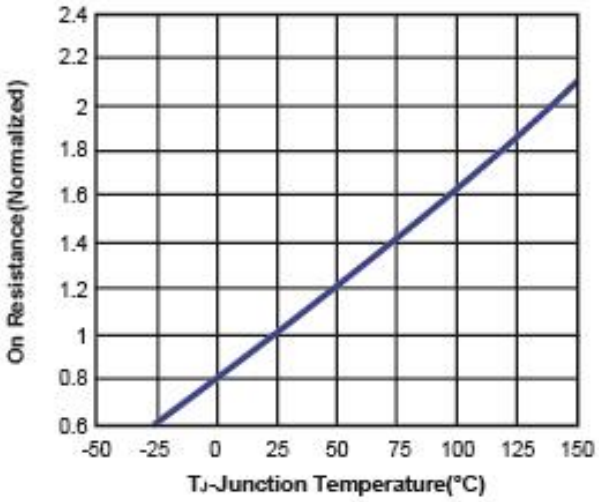
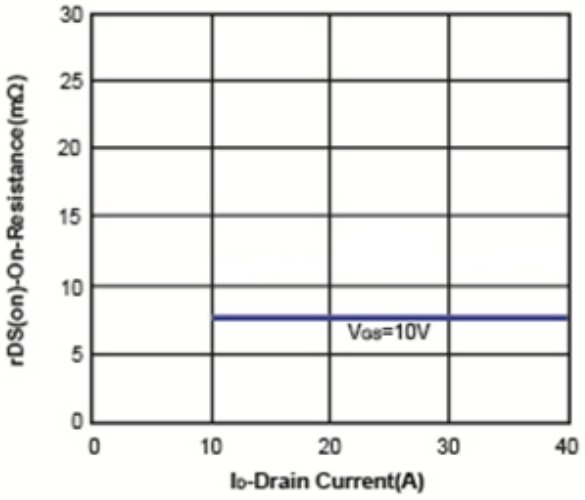
Typical Characteristics (T_J =25℃ Noted)

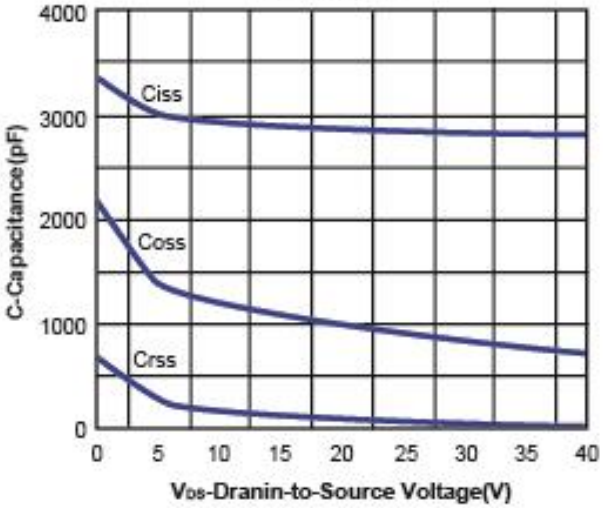
On Resistance vs. Junction Temperature



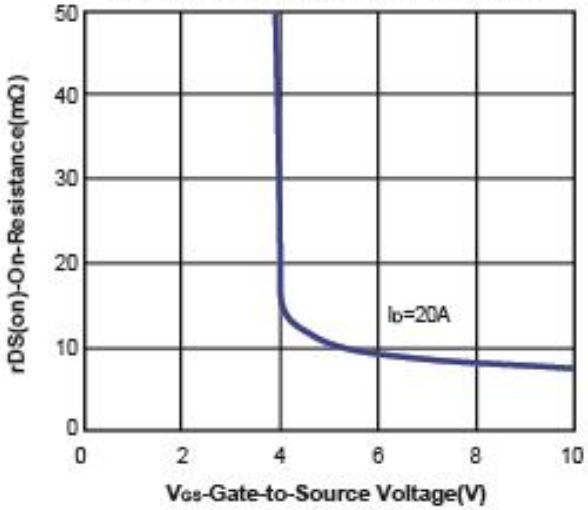
On Resistance vs. Drain Current



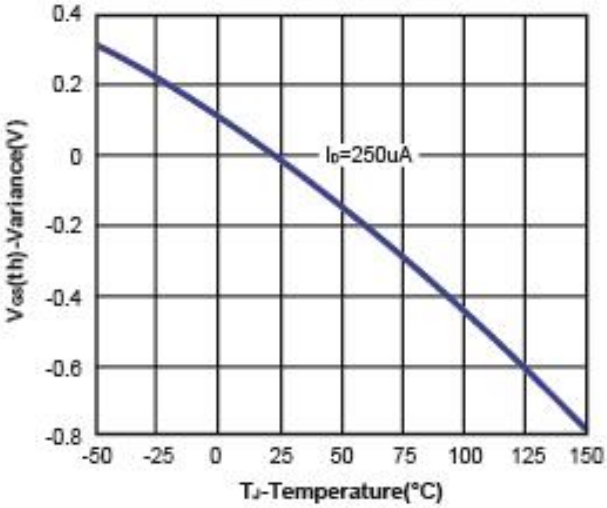
Capacitance



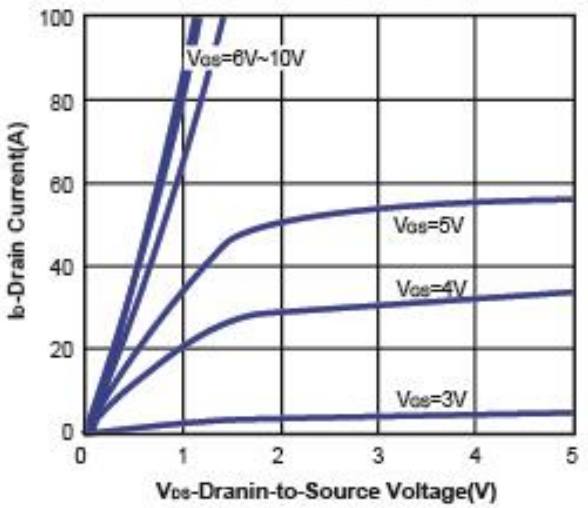
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



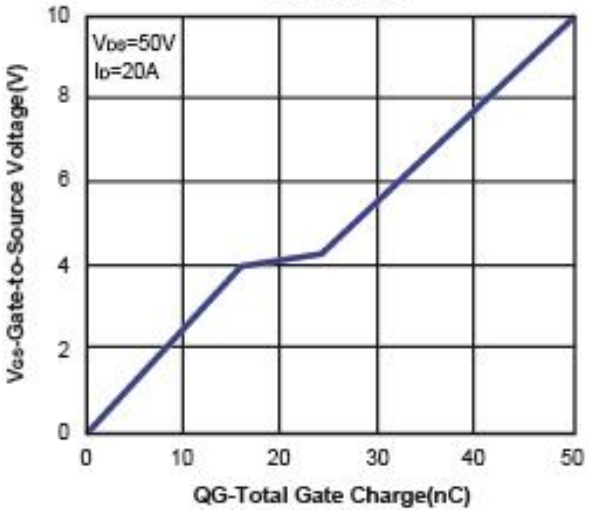
On-Region Characteristics



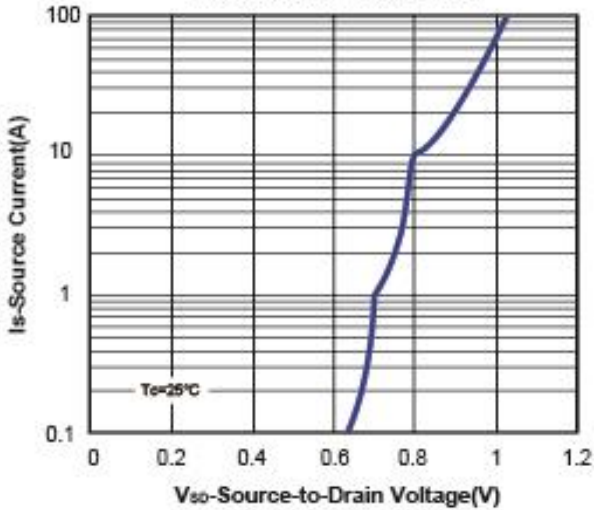
N-Channel 100V(D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

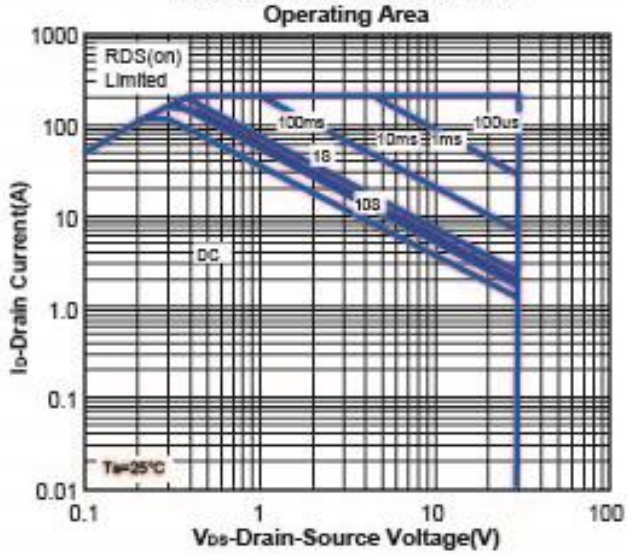
Gate Charge



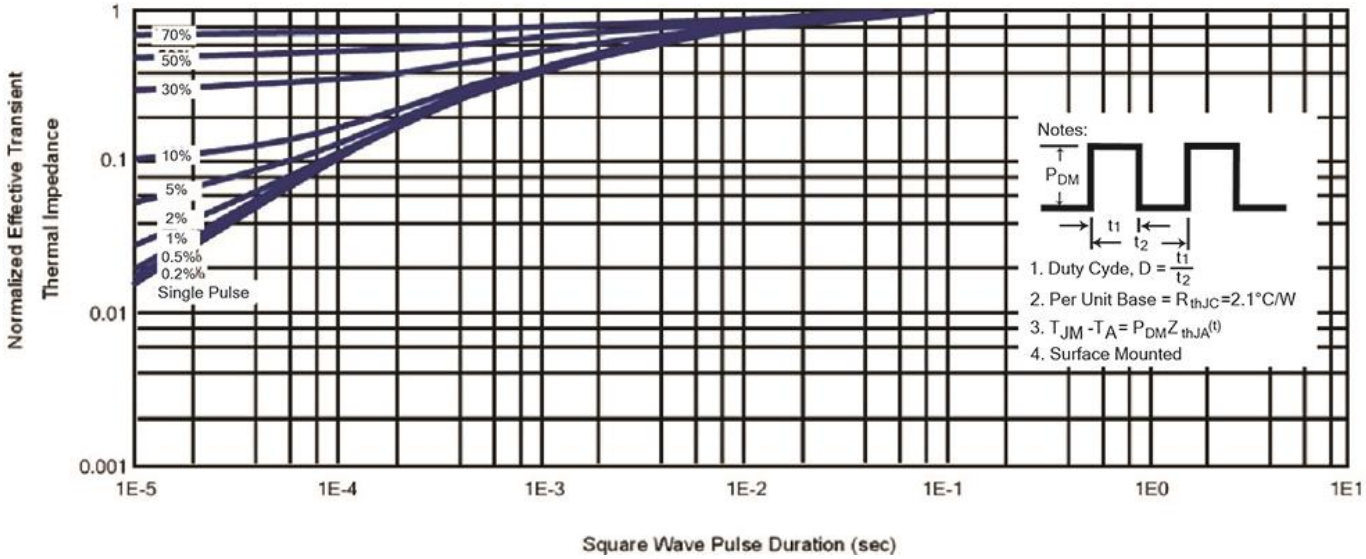
Body-diode characteristics



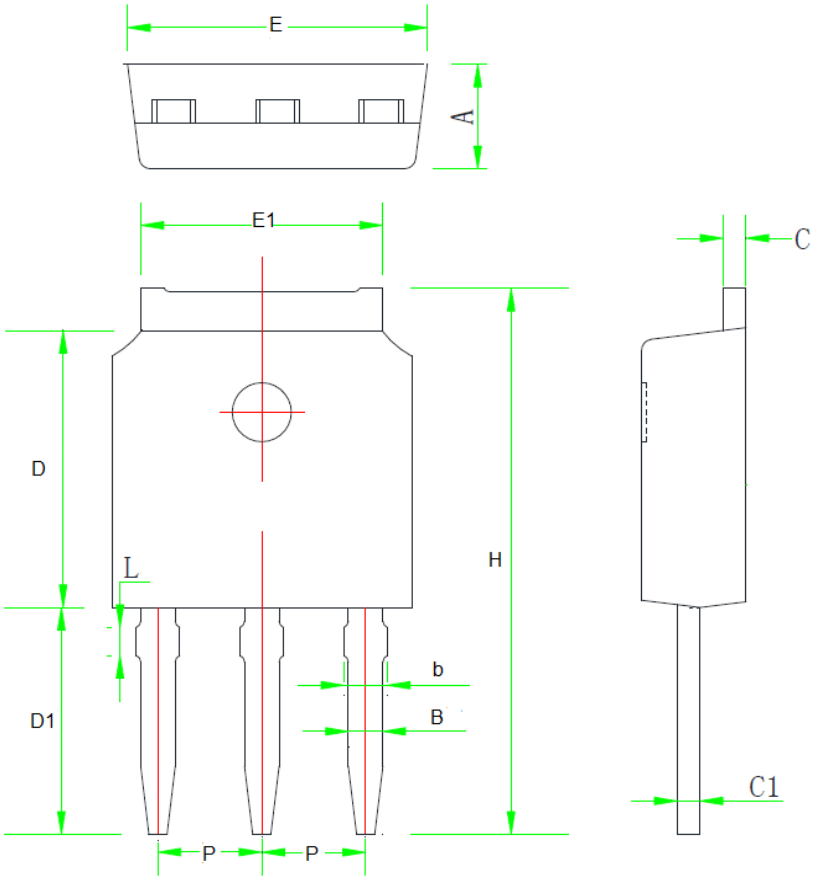
Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



TO-251 Package Outline



SYMBOL	MILLIMETERS(mm)	
	MIN	MAX
A	2.00	2.60
B	0.40	0.91
b	0.65	1.15
C	0.35	0.66
C1	0.35	0.67
D	5.30	6.50
D1	3.30	5.50
H	10.20	12.62
E	6.30	6.90
E1	4.80	5.64
L	0.6 BSC	
P	2.30 BSC	